IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): An image processing apparatus comprising:

~~a sensor board unit arranged~~ an image unit configured to ~~receive~~ provide image data based on a scanned original document;

a control unit; and

an arithmetic processing unit configured to receive the image data from the image ~~process image data relating to the image data received by the sensor board~~ unit ~~to provide processed image data representing a reproduction of said original document~~, said arithmetic processing unit including,

a programmable arithmetic processing section ~~of SIMD (Single Instruction Multiple Data stream) type~~ configured to provide simultaneous processing of plural image data portions,

a memory configured with a plurality of addressable memory locations, with each memory location storing image data portions relating to the image data ~~received~~ provided by the ~~sensor board~~ image unit,

a control register section configured to receive control inputs directly from ~~a control unit~~[[,]] said control unit ~~being~~ outside of said arithmetic processing unit, said control register section being further configured to provide control register section outputs based on said control inputs, and

a memory controller section configured to be responsive to the control register section outputs to control ~~access to at least some of said addressable memory locations to control transfer of the image data portions stored thereat to said programmable arithmetic processing section depending on types of said simultaneous processing to provide said plural image data portions undergoing said simultaneous~~

~~processing to provide said processed image data representing the reproduction of said original document~~ selection of one data transfer mode from a plurality of data transfer modes available to provide different data transfer operations between the arithmetic processing unit and the memory, said transfer modes including at least a random access transfer mode in which a memory address must be included to access the memory for said data transfer and at least one other data transfer mode[[;]] ~~and an image writing unit arranged to receive and use said processed image data representing the reproduction of said original document to produce a second document~~.

Claim 2 (Canceled).

Claim 3 (Currently Amended): The image processing apparatus according to claim [[2]] 1, wherein said ~~control register section is configured to provide a control register section output to control changes between a random access~~ at least one other data transfer mode ~~in which an address~~ is ~~set to access the memory and~~ an automatic access mode in which an address is automatically updated to access the memory.

Claim 4 (Currently Amended): The image processing apparatus according to claim [[2]] 1, wherein said ~~control register section is configured to provide a control register section output to read~~ at least one other data transfer mode is a redundant transfer mode in which data is transferred redundantly from a single addressable memory location of said memory and to ~~provide a control register section output to set a redundant readout transfer mode to configure the memory controller section to transfer the redundantly read data to said arithmetic processing section, such that~~ a plurality of processing elements in said arithmetic processing section ~~receive the redundantly read data from the single addressable memory location~~.

Claim 5 (Currently Amended): The image processing apparatus according to claim [[2]] 1, wherein said ~~control register section is configured to provide a control register section output to control the memory controller section to read data from said arithmetic processing section by thinning out and to provide a control register section output to set~~ at least one other data transfer mode is a ~~thinning-out read~~ transfer mode ~~for transferring~~ in which data provided from the arithmetic processing section is thinned out prior to transfer to said memory.

Claim 6 (Currently Amended): An image processing apparatus comprising:

~~a sensor board~~ means for ~~receiving~~ providing image data based on a scanned original document;

control means; and

an arithmetic processing means for receiving ~~performing processing of image data relating to~~ the image data ~~received by~~ from the ~~sensor board~~ means for providing ~~to provide~~ ~~processed~~ image data ~~representing a reproduction of said original document~~, said arithmetic processing means including,

a programmable arithmetic processing means ~~of SIMD (Single Instruction Multiple Data stream) type~~ for ~~performing~~ simultaneous processing ~~of~~ plural image data portions,

memory means having a plurality of addressable memory locations, with each memory location storing image data portions relating to the image data ~~received~~ provided by the ~~sensor board~~ means for providing image data,

a control register means for receiving control inputs directly from ~~a separate control means~~[[,]] said ~~separate~~ control means ~~being~~ external to said arithmetic

processing means, said control register means further processing said control inputs to

provide control register means outputs, and

a memory controller means for controlling ~~access to at least some of said~~

~~addressable memory locations in response to the control register means outputs to~~

~~control~~ selection of one data transfer mode responsive to ~~of the image data portions~~

~~stored thereat to~~ said control register means outputs, ~~programmable arithmetic~~

~~processing means as~~ said selection of one data transfer mode being made from a

plurality of data transfer modes available to provide different data transfer operations

between the arithmetic processing unit and the memory, said transfer modes including

at least a random access transfer mode in which a memory address must be included

to access the memory for said data transfer and at least one other data transfer mode

~~plural image data portions undergoing said simultaneous processing to provide said~~

~~processed image data representing the reproduction of said original document~~[[;]] ~~and~~

~~image writing means for receiving and using said processed image data representing~~

~~the reproduction of said original document to produce a second document.~~

Claim 7 (Canceled).

Claim 8 (Currently Amended): The image processing apparatus according to claim

[[7]] 6, wherein said ~~control register means provides a control register means output to~~

~~control changes between a random access~~ at least one other data transfer mode ~~changes~~

~~between a random access mode in which an address~~ is ~~set to access the memory and~~ an

automatic access mode in which an address is automatically updated to access the memory

means.

Claim 9 (Currently Amended): The image processing apparatus according to claim 7,

wherein said ~~control register means provides a control register means output to control the~~

~~memory controller means to read~~ at least one other data transfer mode is a redundant transfer

mode in which data is transferred redundantly from a single addressable memory location of

said memory ~~means and provides a control register means output~~ to ~~set a redundant readout~~

~~transfer mode to control the memory controller section for transferring the redundantly data~~

~~to said arithmetic processing means, such that~~ a plurality of processing elements in said

arithmetic processing means ~~receive the redundantly read data from a the single addressable~~

~~memory location.~~

Claim 10 (Currently Amended): The image processing apparatus according to claim

[[7]] 6, wherein said ~~control register means provides a control register means output to~~

~~control the memory controller means to read data from said arithmetic processing mean by~~

~~thinning out and provides a control register means output to set~~ at least one other data transfer

mode is a ~~thinning-out read~~ transfer mode ~~for transferring~~ in which data provided from the

arithmetic processing means is thinned out prior to transfer to said memory means.

Claim 11 (Currently Amended): An image processing method ~~to be~~ executed by an

image processing apparatus, said image processing apparatus including a programmable

~~SIMD type~~ arithmetic image processing section for simultaneous processing a plurality of

image data portions, each image data portion being digital signals prepared based on a

scanned document image, and a memory having a plurality of addressable memory locations

accessible by a memory controller section to provide image data stored at said plurality of addressable memory locations as image data portions related to the scanned document image to said arithmetic processing section as said plurality of image data portions for simultaneously processing, the method comprising steps of:

receiving data representing said scanned document image ~~from a sensor board unit~~;

receiving control inputs directly from a control unit at a control register section, said control unit being external to said arithmetic <u>image</u> processing section;

processing said control inputs at said control register section to provide control register section outputs to the memory controller section;

controlling <u>selection of a</u> transfer <u>mode from a plurality of transfer modes available to provide different data transfer operations between the arithmetic processing unit and the memory, said transfer modes including at least a random access transfer mode in which a memory address must be included to access the memory for said data transfer and at least one other data transfer mode,</u> ~~of at least some of the image data portions related to the scanned document image between~~ said ~~addressable memory locations and said arithmetic processing section~~ selection being performed by using said memory controller section under control of said control register section outputs, ~~and controlling transfer of processed data from said programmable arithmetic processing section to provide a processed reproduction of said scanned document image; and~~

~~transferring the processed reproduction of said scanned document image to a second document.~~

Claim 12 (Canceled).

Claim 13 (Currently Amended): The image processing method according to claim 11,

wherein said ~~controlling transfer step includes changing between a random access~~ at least one

other data transfer mode ~~in which an address~~ is ~~set to access the memory, and~~ an automatic

access mode in which an address is automatically updated to access the memory[[,]] ~~in~~

~~accordance with one of the control inputs provided from outside~~.

Claim 14 (Currently Amended): The image processing method according to claim 11,

wherein said ~~controlling transfer step includes reading data redundantly from a single~~

~~memory address of said memory, in accordance with one of the control inputs provided from~~

~~outside, and setting~~ at least one other data transfer mode is a redundant readout transfer mode

for transferring the redundantly read data portions from a single address of the memory to

~~said arithmetic processing section, such tha~~t a plurality of processing elements in said

arithmetic processing section ~~receive said redundantly read data from a the single memory~~

~~address~~.

Claim 15 (Currently Amended): The image processing method according to claim 11,

wherein said ~~controlling transfer step includes reading data portions from said arithmetic~~

~~processing section by thinning out, in accordance with one of the control inputs provided~~

~~from outside, and setting~~ at least one other data transfer mode is a ~~thinning out read~~ transfer

mode ~~for transferring~~ in which data provided from the arithmetic processing section is

thinned out prior to transfer to said addressable memory locations in said memory.

wherein said ~~controlling transfer step includes reading data portions from said arithmetic processing section by thinning out, in accordance with one of the control inputs provided from outside, and setting~~ at least one other data transfer mode is a ~~thinning-out read~~ transfer mode ~~for transferring~~ in which data provided from the arithmetic processing section is thinned out prior to transfer of the data portions to the addressable memory locations of said memory.

Claim 16 (Currently Amended): A computer readable medium for storing instructions, which when executed by a computer, causes the computer to perform an image processing method ~~to be~~ executed by an image processing apparatus, said image processing apparatus including a programmable ~~SIMD type~~ arithmetic image processing section for simultaneous processing a plurality of image data portions, each image data portion being digital signals prepared based on a scanned document image, and a memory having a plurality of addressable memory locations accessible by a memory controller section to provide image data stored at said plurality of addressable memory locations as image data portions related to the scanned document image to said arithmetic processing section as said plurality of image data portions for simultaneously processing, the method comprising steps of:

receiving data representing said scanned document image ~~from a sensor board unit~~;

receiving control inputs directly from a control unit at a control register section, said control unit being external to said arithmetic <u>image</u> processing section;

processing said control inputs at said control register section to provide control register section outputs to said memory controller section;

controlling <u>selection of a</u> transfer <u>mode from a plurality of transfer modes available to provide different data transfer operations between the arithmetic processing unit and the</u>

memory, said transfer modes including at least a random access transfer mode in which a memory address must be included to access the memory for said data transfer and at least one other data transfer mode, ~~of at least some of the image data portions related to the scanned document image between~~ said ~~addressable memory locations and said arithmetic processing section~~ selection being performed by using said memory controller section under control of said control register section outputs, ~~and controlling transfer of processed data from said programmable arithmetic processing section to provide a processed reproduction of said scanned document image; and~~

~~transferring the processed reproduction of said scanned document image to a second document.~~

Claim 17 (Previously Presented): The image processing apparatus according to claim 1, further comprising an image data control unit arranged to expand an image area of said image data.

Claim 18 (Previously Presented): The image processing apparatus according to claim 17, wherein said image data control unit is arranged to scale said image data.

Claim 19 (Previously Presented): The image processing apparatus according to claim 17, wherein said image data control unit is arranged to synthesize a plurality of sets of image data.

Claim 20 (Previously Presented): The image processing apparatus according to claim 19, wherein at least one of said plurality of sets of image data is communicated to said image processing apparatus from another apparatus.